Amendments to the Claims

1-2. (canceled)

3. (currently amended) A dynamic domino circuit ~~The dynamic adder of claim 2, further~~ comprising:

a logic portion adapted for processing logic of said dynamic domino, circuit;

a first dynamic output portion coupled to said logic portion, said first dynamic output portion having a first dynamic node for dynamically holding a first data;

a second dynamic output portion coupled to said logic portion, said second dynamic output portion having a second dynamic node for dynamically holding a second data;

a third dynamic output portion coupled to said logic portion, said third dynamic output portion having a third dynamic node for dynamically holding a third data;

a first and a second transistors having their gates coupled to said first dynamic node, said first transistor having its drain coupled to said second dynamic node, said second transistor having its drain coupled to said third dynamic node;

a third and a fourth transistors having their gates coupled to said second dynamic node, said third transistor having its drain coupled to said first dynamic node, said fourth transistor having its drain coupled to said third dynamic node; and

a fifth and a sixth transistors having their gates coupled to said third dynamic node, said fifth transistor having its drain coupled to said first dynamic node, said sixth transistor having its drain coupled to said second dynamic node; and

a multiplexer coupled to a final stage comprising:

(a) a latch built into said multiplexer; and

(b) a first and a second dynamic select inputs to said multiplexer, wherein said multiplexer functions as a latch using said latch when said first and said second dynamic select inputs are precharged to logic zero, and wherein said multiplexer functions as a multiplexer when said first and said second select inputs are evaluated to their respective logic values.

4-6. (canceled)

7. (currently amended) A dynamic adder to generate dynamic logic inversions comprising: ~~The dynamic adder of claim 4,~~

a dynamic circuit implementing a mutually exclusive circuit to compute a three terms carry logic, wherein the value of each of the three terms carry logic is represented as a dynamic output computed as a function of true terms;

wherein the mutually exclusive circuit includes three dynamic output portions representing one for each of the three terms carry logic where each dynamic output portion is coupled to gates of transistors whose drains are coupled to the other dynamic output portions such that the output of a selected dynamic output portion is exclusive of the values of the other dynamic output portions; and

wherein groups of said three terms carry logic compromises group propagate (gp), group generate (gg), and group kill (gk).

8. (previously presented) The dynamic adder of claim 7, wherein the groups of said three terms carry logic are mutually exclusive.

9. (previously presented) The dynamic adder of claim 8, wherein the inversion is implemented by (~gk)=(gp)+(gg).

10. (previously presented) The dynamic adder of claim 8, wherein the inversion is implemented by (~gp)=(gg)+(gk).

11. (previously presented) The dynamic adder of claim 8, wherein the inversion is implemented by (~gg)=(gp)+(gk).

12-16. (canceled)